REMARKS

Claims 1, 2, 4, 8-10, 25 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Kim (U.S. Patent Number 6,215,791) and claims 11-14, 16-22, 26, 29 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Kim and further in view of Waclawsky (U.S. Patent Number 6,449,255). The Examiner's thoughtful and thorough reply in the *Response to Arguments* section of the present office action is appreciated. However, the applicants respectfully disagree with these rejections and request reconsideration.

Independent claims 1 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Kim (U.S. Patent Number 6,215,791). Independent claim 1 recites "inserting a time-delay indication into a portion of the first information packet, the time-delay indication corresponding to the period of time that the first information packet **was stored in the router.**" Independent claim 25 recites "inserting a time-delay indication into a portion of the information packet, the time-delay indication corresponding to the period of time that the information packet **was stored in the router.**"

The Examiner asserts that the applicants do not expressly disclose as prior art this claim language. (See pages 4, 5 and 8 of the present office action.) The applicants agree and submit that they do not even suggest functionality described by this claim language. However, the Examiner does cite the entire background section of the present application. Page 1, line 16 – page 4, line 12 reads as follows:

> Full duplex wireless communication systems are well known and include various types of systems, such as cellular telephone systems, personal communication systems, integrated systems, such as the "MOTOROLA" "iDEN" system, and real-time video systems. Such wireless systems are known to include a system infrastructure and communication devices constructed and programmed to operate in the respective system. The system infrastructure includes fixed network equipment, such as base transceiver sites (BTSs), system controllers (e.g., base site controllers (BSCs)), switching centers, routers, communication links, antenna towers, and various other known infrastructure components.
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> Certain wireless communication systems, such as digital cellular systems and the "MOTOROLA" "iDEN" system utilize voice compression techniques, such as vector sum-excited linear predictive (VSELP) encoding, advanced multi-band excitation (AMBE) encoding or code-excited linear predictive

(CELP) encoding, to more efficiently utilize available frequency spectrum. In such systems, each BSC and each wireless communication device include one or more transcoders that encode (compress) pulse code modulated (PCM) or other digitally sampled voice signals received from the audio portion of the infrastructure (e.g., from a mobile switching center (MSC)) or communication device, respectively, and decode (decompress) received compressed voice signals received from the radio frequency portion of the infrastructure (e.g., BTS) or communication device, respectively. Each transcoder includes one or more digital signal processors (DSPs) and associated control circuitry and operating software. With current DSP technology, each DSP can support one or more two-way, full duplex audio communications.

To compress incoming PCM audio signals, the infrastructure transcoder typically encodes a predetermined amount of audio and packetizes the encoded audio to comply with the transmission format of the outgoing communication link. The amount of audio encoded by the transcoder corresponds to the radio transmission access protocol employed by the BTS. For example, the BSC transcoder of the "iDEN" system VSELP encodes ninety (90) milliseconds (ms) of audio in two forty-five (45) millisecond transmission frames or three thirty (30) millisecond transmission frames (depending on whether the BTS transmission rate is full rate or half rate) and packetizes the transmission frames into a single information packet in accordance with a high data level link control (HDLC) protocol utilized on the communication link between the BSC and its associated BTSs. The "iDEN" BTS employs a time division multiple access (TDMA) transmission protocol in which each time slot supports ninety (90) milliseconds of information (compressed audio or data). Therefore, the ninety milliseconds of compressed audio in each HDLC information packet coincides with the amount of compressed audio that may be transmitted from the BTS in a single time slot.

The timing at which the BSC communicates compressed transmission frames to a BTS also depends on the particular radio transmission access protocol employed by the BTS. Such timing is particularly important when the access protocol is time-based, such as the TDMA protocol utilized in the "iDEN" system and other digital cellular systems (e.g., the Global System for Mobile Communications (GSM)). For proper transmission from a BTS that utilizes a TDMA protocol, the BTS and BSC must be synchronized such that the BSC conveys an information packet, which my include multiple transmission frames, to the BTS prior to the beginning of the transmission time slot allocated for transmitting the packet. Optimally, the packet should arrive at the BTS just early enough to enable the BTS to process the packet (e.g., modulate, filter, upconvert, and amplify) before the beginning of the transmission time slot to minimize the amount of buffering or storage of compressed audio that must occur at the BTS and, therefore, minimize the gaps or choppiness in audio perceived by the user of the recipient communication device.

However, due to various delay mechanisms within the infrastructure, and even within the transcoders themselves, a fixed synchronization between BSC and BTS is not possible. Therefore, BSCs and BTSs typically employ a synchronization protocol in an attempt to maintain synchronization in view of the various delays. Under such protocols, the BTS instructs the BSC to adjust its packet transmission time based on the historical arrival of information packets from the BSC for a particular communication.

BSCs typically service multiple BTSs in full duplex wireless systems. Consequently, each BSC commonly includes a router that directs encoded audio from the transcoder to the appropriate BTS. When a deterministic transport protocol, such as a circuit-switched protocol, is used between the router and the BTS, the router introduces a determinate, but not necessarily fixed, delay which can be taken into account by the BTS when instructing the BSC to transmit a particular information packet in accordance with the synchronization protocol. However, packet switching is becoming more popular these days to increase the effective bandwidth of the communication path between the BSC and the BTS.

When a packet-switched transport protocol is used to communicate information from the BSC to the BTS, the delays introduced by the router become non-deterministic and may produce wide variances in arrival times of information packets at the BTS. In an attempt to account for such wide variances, prior art BTSs estimate the router delay and request transmission of packets from the transcoder based on the estimate in accordance with their respective synchronization protocols. However, notwithstanding such estimation by the BTS, the nondeterministic nature of the BSC-to-BTS transport can result in receipt of a packet by

> the BTS after the BTS transmission time for the packet has expired. That is, the indeterminate delays of the router in a nondeterministic system can result in missed packet transmissions and poor signal quality (e.g., choppy audio) as perceived by a user of a wireless communication device.
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> In addition to introducing variable delays, a non-deterministic packetized transport employed between the BSC and the BTS provides no order with which the router transmits packets received from the transcoder. Such a lack of order can introduce undesirable delays, and therefore poor perceived signal quality, in communications in which synchronization between the BSC and BTS is already established. For example, if the router receives a packet for a first full-duplex communication that is just commencing and in which synchronization is not yet established between the BSC and the BTS, and another packet for a second full-duplex communication that is ongoing and in which synchronization has been established between the BSC and the BTS, the router may communicate the first communication's packet to the BTS before communicating the second communication's packet, thereby introducing an undesired delay in the conveyance of the second communication's packet and degrading perceived quality of the second communication.
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> Therefore, a need exists for a method and apparatus for improving signal quality of transmitted information as perceived by a user of a wireless communication device that accounts for variable delays introduced by a BSC's router when a non-deterministic packetized transport is used to communicate information between the router and the BTS, and that appropriately prioritizes transmissions from the BSC to its respective BTSs to minimize delays and thereby substantially improve the quality of communications as perceived by users of recipient wireless communication devices.

The Examiner also asserts that the applicants do "disclose as prior art transmitting packets based upon delays where the delays are based on a status of synchronization of the transcoder transmission time and the base transceiver site transmission time." (See pages 5, 8 and 9 of the present office action.) The applicants submit that this assertion as a very broad statement and are unclear upon what language in the background section quoted above the Examiner is specifically relying.

In addition to the applicants' background section, the Examiner cites Kim column 5 lines 26-50 and column 6 lines 15-22 as teaching the portions of claims 1 and 25 quoted above. To provide some context for the Examiner's citations, Kim column 5 line 26 - column 6 lines 45 is quoted as follows (emphasis added):

> FIG. 6 illustrates **a priority-address pair** in accordance with the present invention. A priority field bisects itself into areas for a deadline time and for an eligible time, respectively. The deadline time can be defined as a **maximum allowable delay bound at a node** in a broadband integrated service digital network (B-ISDN). The deadline time at a node is determined on condition that the sum of all the deadline times cannot exceed a source-to-destination delay bound. If a cell under transmission exceeds the deadline time at a node, the end-to-end bound may not be kept, thereby the cell being regarded as useless. The eligible time refers to a **delay bound in which a cell is supposed to be transmitted from a node**, being determined by taking account of a jitter. It is defined by a following mathematical formula.
>
> [Mathematical Formula]
> $ET\,i,j^{k}=ET\,i-1,j^{k}+d\,i-1,j+t\,i,$

wherein, the ET i,j^k denotes an eligible time assigned to a cell k for a channel j at a node i; the ET $i\text{-}1,j^k$ denotes an eligible time assigned to the cell k for the channel j at a node i-1; the d i-1,j represents a deadline time for the channel j at the node i-1; and the t i refers to a propagation delay between the node i-1 and the node i. The above formula represents that the eligible time of cell k at node i depends on the eligible time and the deadline time of the previous node i-1.

A queue management system in accordance with the present invention handling the above described priority-and-address pair can be implemented with a system, which has substantially same contour as the prior art system. Accordingly, the inventive structures and operations of a TDM 31 , a cell pool 32 , an idle-address FIFO 34 , a write controller 35 and a read controller 36 in the present invention are identical to those of the blocks with same numerals in the prior art system in FIG. 3 .

FIG. 7 describes detailed building blocks of **an inventive sequencer** capable of controlling the jitter. In the inventive sequencer, a module 70 is repeated side-by- side. The number of modules incorporated in the inventive sequencer is equal to the number of cells being storable in the cell pool 32 . Each module 70 includes a controller 71 , a register 72 , a comparator 73 and a selector 74 .

The priority field including the eligible time and the deadline time is stored in the register 72 . Addresses in the cell pool 32 are also stored in the register 72 , wherein each address designates a section in the cell pool 32 in which a cell associated with the priority field is stored. A real time and the eligible time are asserted to the comparator 73 . The selector 74 selectively yields one between an output from a left-hand side selector and the address in the register 72 . The controller 71 compares the priority field of the corresponding module 70 with that of a left-hand module denoted by a subscript i-1, and also with that of a new entry. Then, the controller 71 chooses a priority-and address pair as a result of the comparison, and finally let the register 72 store the chosen priority-and-address pair.

The sequencer in accordance with the present invention sequentially compares first the deadline time of a new entry with that of the entries the sequencer has been keeping. An entry with smaller value of the deadline time is arranged right-side of an entry with larger deadline time. In case that the deadline times are same, the eligible times are compared, and then, an entry with a smaller value of the eligible time is arranged to be at the right-side than an entry with larger eligible time.

In contrast to the conventional queue management system, the inventive queue management system provides a priority based not only on the deadline time but also on the eligible time. More specifically, after the real time and the eligible time in each module are compared, a cell having the eligible time smaller than the real time is served first. Among the cells with eligible time smaller than the real time, a cell with a smaller eligible time is served first.

The comparator 73 compares the real time with the eligible time stored in the register 72 . If the eligible time ET i of a cell is larger than the real time, i.e., if the cell arrives earlier than the eligible time, the selector 74 selects the output of the left-hand selector; but if the eligible time is smaller than the real time, the selector 74 selects the address A i . stored in the register 72 .

The queue management system in accordance with the present invention is designed such that even a cell with high priority resulted from a small value of the deadline time is not supposed to be served until the arrival of the eligible time. Consequently, any cell is not allowed to be served until the arrival of the eligible time, which, in turn, makes a significant contribution in controlling the jitter.

Thus, Kim appears to teach time requirements, the deadline time and the eligible time for the cell, that are "assigned" to a node rather than indications of times for which one or more packets are actually stored by a router. This is a fundamentally different approach than what is presently claimed. The applicants fail to see where or how Kim

teaches or even suggests anything about how long a packet **WAS already stored.**

For the purpose of argument, consider the Examiner's earlier assertion as true, that the applicants do "disclose as prior art transmitting packets based upon delays where the delays are based on a status of synchronization of the transcoder transmission time and the base transceiver site transmission time." (See pages 5, 8 and 9 of the present office action.) Now add to this the teaching of Kim regarding a queue management system and/or sequencer that utilize Kim's priority-and-address pair (i.e., the deadline time and the eligible time). The Examiner asserts that the applicants' "admitted prior art in view of Kim suggests that the **time-delay indication** is used by the base transceiver site to synchronize transcoder transmission time to the base transceiver site transmission time" (emphasis added). However, the applicants submit that the time-delay indication is Kim's deadline time and eligible time, since neither Kim nor the applicants' admitted art suggest that the time-delay indication corresponds to **the time one or more packets were stored in the router.**

In the *Response to Arguments* section of the present office action, the Examiner suggests that the "corresponding to" language in the claims is sufficiently broad to encompass the teachings of Kim's deadline time and eligible time as *corresponding to* the period of time that the first information packet was stored in the router. While the applicants acknowledge that the "corresponding to" language is relatively broad, the applicants submit that Kim's deadline time and eligible time do not correspond to the time one or more packets **were already** stored in the router. Kim's deadline time and eligible time refer to how a cell **should be processed**, not how a packet **was processed already.** The applicants have used the "corresponding to" language in order to generically capture the many possibilities for conveying the time-delay indication. Allowed claims 5-7, 15, 23, 28 and 31 represent some of these possibilities.

Claims 11, 19 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Kim and further in view of Waclawsky (U.S. Patent Number 6,449,255). Independent claim 11 recites, "the indication of the desired transcoder transmission time being based on a period of time that at least one prior information packet of the first communication **was stored in the router.**" Independent claim 19 recites "receiving an information packet from the router,

the information packet including a time-delay indication, and the time-delay indication corresponding to a period of time that the information packet **was stored in the router.**" Independent claim 29 recites "receiving an indication of a desired transcoder transmission time for the additional information packet, the indication being based on a period of time that the at least one information packet of the first group of information packets **was stored in the router.**" Thus, these independent claims also refer to an indication of a period of time for which a packet is actually stored by the router. The applicants submit that all of the arguments above with respect to claims 1 and 25 also apply to claims 11, 19 and 29. Furthermore, the applicants submit that Waclawsky does not teach or suggest these claim portions.

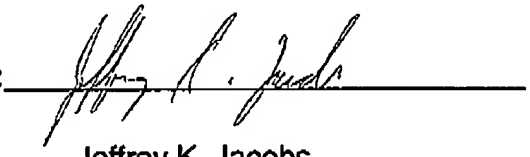
In the *Response to Arguments* section of the present office action, the Examiner suggests that claims 11 and 29 only require that the base transceiver site determine the transcoder transmission time based on the packet delay time and that the applicants do not require that the packets sent through the router contain the time the packet was actually stored in the router. Claim 11 recites, "**receiving an indication** of a desired transcoder transmission time for the information packet, the indication of the desired transcoder transmission time being **based on a period of time that at least one prior information packet of the first communication was stored in the router.**" Claim 29 recites "**receiving an indication** of a desired transcoder transmission time for the additional information packet, the indication being **based on a period of time that the at least one information packet of the first group of information packets was stored in the router.**" Thus, the applicants do not agree with the Examiner's characterization of these claims. These claims do not "only require that the base transceiver site determine the transcoder transmission time based on the packet delay time." (See page 2 of the present office action.) Clearly, each recite receiving an indication that is based on the time one or more packets **were already stored in the router**. Again, as discussed at length above, the applicants submit that the cited art does not teach or suggest this claim language.

Since none of the references cited, either independently or in combination, teach all of the limitations of the independent claims, or therefore, all the limitations of their respective dependent claims, it is asserted that neither anticipation nor a prima facie

case for obviousness has been shown. No remaining grounds for rejection or objection being given, the claims in their present form are asserted to be patentable over the prior art of record and in condition for allowance. Therefore, allowance and issuance of this case is earnestly solicited.

The Examiner is invited to contact the undersigned, if such communication would advance the prosecution of the present application. Lastly, please charge any additional fees (including extension of time fees) or credit overpayment to Deposit Account No. **502117 -- Motorola, Inc.**

Respectfully submitted,
M. Bychowsky et al.

By: 

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